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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,264	WOLCZKO ET AL.	
	Examiner	Art Unit	
	ANDREW CHOU	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 8, 14, and 18 are amended. Claims 1-22 are pending.

Information Disclosure Statement

2. The Office acknowledges receipt of the Information Disclosure.Statement filed on 12/20/2007. It has been placed in the application file and the information referred to therein has been considered by the examiner.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 18-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 18 is non-statutory as being "a sampling mechanism for sampling an instruction executing in a multi-threaded processor comprising...sampling logic...sampling register logic...instruction history registry logic...sample filtering...", thus the sampling mechanism is not yet embodied in executable code format as a computer component. Thus, the computer program product is computer listings *per se*, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being

performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer- readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Accordingly, it is important to distinguish claims that define descriptive material per se from claims that define statutory inventions. MPEP 2106.01 (I)

Response to Arguments

5. Applicant's arguments filed 12/05/2007 have been fully considered but they are not persuasive.

On page 6, paragraph 2 of Applicant's Remarks, Applicant argues that Chrysos et al. No. 6,000,044 does not disclose the limitation "reporting the sampling information to the particular thread when the sampling information includes an event of interest", as stated in claim 1. Examiner respectfully disagrees and would like to direct Applicant's attention to Chrysos column 10, lines 5-19, where Chrysos discloses reporting information that is determined to be interesting and useful.

On page 6, paragraph 3 of Applicant's Remarks, Applicant argues that Chrysos does not disclose the limitation of Claim 8, "decrementing the candidate counter when all events for the instruction have occurred...". Examiner disagrees and respectfully

points to Chrysos column 14, line 64-66, "...decrementing...", FIG. 2B, item 510, "counter", and column 15, lines 5-15, where in an alternative embodiment the counter is decremented after every cycle, or when all events for an instruction has occurred.

On page 7, paragraph 3 of Applicant's Remarks, Applicant argues that Chrysos does not disclose the limitation of Claim 18, wherein the sampling register logic, sample filtering and counting logic is replicated on a per thread basis". Examiner respectfully disagrees and would like to direct Applicant's attention to column 26, lines 56-65, "With the present sampling, it is possible to determine how each thread uses each class..." and FIG. 14b, item 1480.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Chrysos et al. US 6,000,044 (hereinafter Chrysos)

Claim 1:

A method of sampling instructions executing in a multi-threaded processor comprising:

selecting an instruction for sampling (see for example column 6, lines 40-45);

storing sampling information relating to the instruction (see for example column 6, lines 40-45);

determining whether the sampling information includes an event of interest, the event of interest to a particular thread, within which the instruction is executing (see for example column 15, lines 30-35, and column 10, lines 5-19);

and reporting the sampling information to the particular thread when the sampling information includes an event of interest on a per-thread basis (see for example column 6, lines 60-65).

Claim 2:

The method of claim 1 further comprising providing a register with a bit vector representing a plurality of events of interest; and

wherein the determining whether the sampling information includes the event of interest further includes comparing the sampling information relating to the instruction to the bit vector (see for example column 16, lines 52-55).

Claim 3:

The method of claim 2 wherein the comparing is via at least one of a mask operation or a more expressive operation (see for example column 16, lines 52-55).

Claim 4:

The method of claim 1 wherein the selecting the instruction is without regard to a thread to which the instruction is bound (see for example column 6, lines 48-49).

Claim 5:

The method of claim 1 further comprising identifying a thread to which the instruction is bound when the instruction is selected (see for example column 14, lines 53-64).

Claim 6:

The method of claim 1 further comprising providing filtering criteria on a per-thread basis (see for example column 15, lines 21-43, "Filtering Instructions").

Claim 7:

The method of claim 1 further comprising providing a single set of filtering criteria; and, scheduling sampling among a plurality of threads via software (see for example column 15, lines 21-43, "Filtering Instructions).

Claim 8:

A method of sampling instructions executing in a multi-threaded processor comprising:

setting a candidate counter to a number (see for example column 14, lines 64-67);

selecting an instruction for sampling (see for example column 6, lines 40-45);

storing information relating to the instruction (see for example column 6, lines 40-45);

determining whether all events for the instruction have occurred (see for example column 6, lines 40-45);

decrementing the candidate counter when all events for the instruction have occurred and when the instruction corresponds to a desired sampled thread (see for example column 14, line 64-66, "...decrementing...", FIG. 2B, item 510, "counter", and column 15, lines 5-15,);

determining whether the candidate counter equals zero (Chrysos column 15, lines 5-15); and reporting the instruction when the candidate counter equals zero (see for example column 6, lines 60-65).

Claim 9:

The method of claim 8 wherein the information relating to the instruction represents an instruction history (see for example column 6, lines 48-49), and the instruction history includes information relating to at least one of an events value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privilege value, a branch history value and a number in fetch bundle value (see for example column 6, lines 48-49).

Claim 10:

The method of claim 8 wherein the selecting the instruction is without regard to a thread to which the instruction is bound (see for example column 14, lines 53-64).

Claim 11:

The method of claim 8 further comprising identifying a thread to which the instruction is bound when the instruction is selected (see for example column 14, lines 53-64).

Claim 12:

The method of claim 8 further comprising providing filtering criteria on a per-thread basis (see for example column 15, lines 21-34, "Filtering Instructions").

Claim 13:

The method of claim 8 further comprising providing a single set of filtering criteria; and, scheduling sampling among a plurality of threads via software (see for example column 15, lines 21-34, "Filtering Instructions").

Claim 14:

A method of sampling instructions executing in a multi-threaded processor comprising:

setting a candidate counter to a number selecting an instruction for sampling (see for example column 14, lines 64-67);

storing information relating to the instruction (see for example column 6, lines 40-45);

determining whether all events for the instruction have occurred (see for example column 6, lines 40-45);

determining whether the instruction includes events of interest, the events of interest including whether the instruction corresponds to a desired sampled thread (see for example column 15, lines 30-35);

decrementing the candidate counter when all events for the instruction have occurred and when the instruction includes events of interest (column 15, lines 5-15);

determining whether the candidate counter equals zero (see for example column 6, lines 40-45); and

reporting the instruction when the candidate counter equals zero (see for example column 6, lines 40-45);.

Claim 15:

The method of claim 14 further comprising providing a register with a bit vector representing events of interest; and wherein the determining whether the instruction

includes events of interest further includes comparing the information relating to the instruction to the bit vector (see for example column 16, lines 52-55).

Claim 16:

The method of claim 14 wherein the information relating to the instruction represents an instruction history, and the instruction history includes information relating to at least one of an event value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privileged value, a branch history value and a number in fetch bundle value (see for example column 6, lines 48-49).

Claim 17:

The method of claim 14 wherein the selecting an instruction for sampling is based upon sample selection criteria; and the sample selection criteria include information relating to a desired sampled thread (see for example column 15, lines 30-35).

Claim 18:

A sampling mechanism for sampling an instruction executing in a multi-threaded processor comprising:

sampling logic, the sampling logic determining whether the instruction corresponds to a desired sampled thread (see for example column 15, lines 30-35);

sampling register logic coupled to the sampling logic (see for example column 6, lines 40-45);

instruction history register logic coupled to the sampling register logic, the instruction history register logic storing information relating to the instruction (see for example column 6, lines 40-45);

sample filtering and counting logic coupled to the sampling logic see for example column 15, lines 30-42); and

wherein the sample filtering and counting logic is replicated on a per thread basis (see for example column 26, lines 56-65, "With the present sampling, it is possible to determine how each thread uses each class..." and FIG. 14b, item 1480.).

Claim 19:

The sampling mechanism of claim 18 further comprising:

notification logic, the notification logic reporting the information relating to the instruction if the instruction corresponds to the desired sampled thread (see for example column 6, lines 60-65).

Claim 20:

The sampling mechanism of claim 18 wherein the sampling register logic includes a register with a bit vector representing events of interest; and wherein the sampling logic determines whether the instruction includes events of interest by comparing the information relating to the instruction to the bit vector (see for example column 16, lines 52-55).

Claim 21:

The sampling mechanism of claim 18 wherein the information relating to the instruction represents an instruction history (see for example column 6, lines 40-45), and the

instruction history includes information relating to at least one of an events value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privileged value, a branch history value and a number in fetch bundle value (see for example column 6, lines 48-49).

Claim 22:

The sampling mechanism of claim 18 wherein the sampling register logic includes a sample selection criteria register storing sample selection criteria (see for example column 16, lines 52-55); and the sample selection criteria include information relating to a desired sampled thread (see for example column 15, lines 30-35).

Conclusion

8. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto..qov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

AYC

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SUPERVISORY PATENT EXAMINER